TUBF0320 Product Brief

1. Description

The TBUF0320 is a 20-output very-low-power clock buffer for PCIe 1.0/2.0/3.0/4.0/5.0, SAS, SATA, UPI and other applications.

It takes a reference input to fanout twenty 100MHz low-power differential HCSL outputs with on-chip terminations(integrated terminations for 85Ω transmission lines) that can save 80 external resistors and make layout easier.OE pins combined with SMBus bits, as well as a 3-wire side band interface, provide easier power management for each output. All OE pins are power down tolerant, which allows the OE pins to be driven by external signals when the device is in a power down or reset condition.

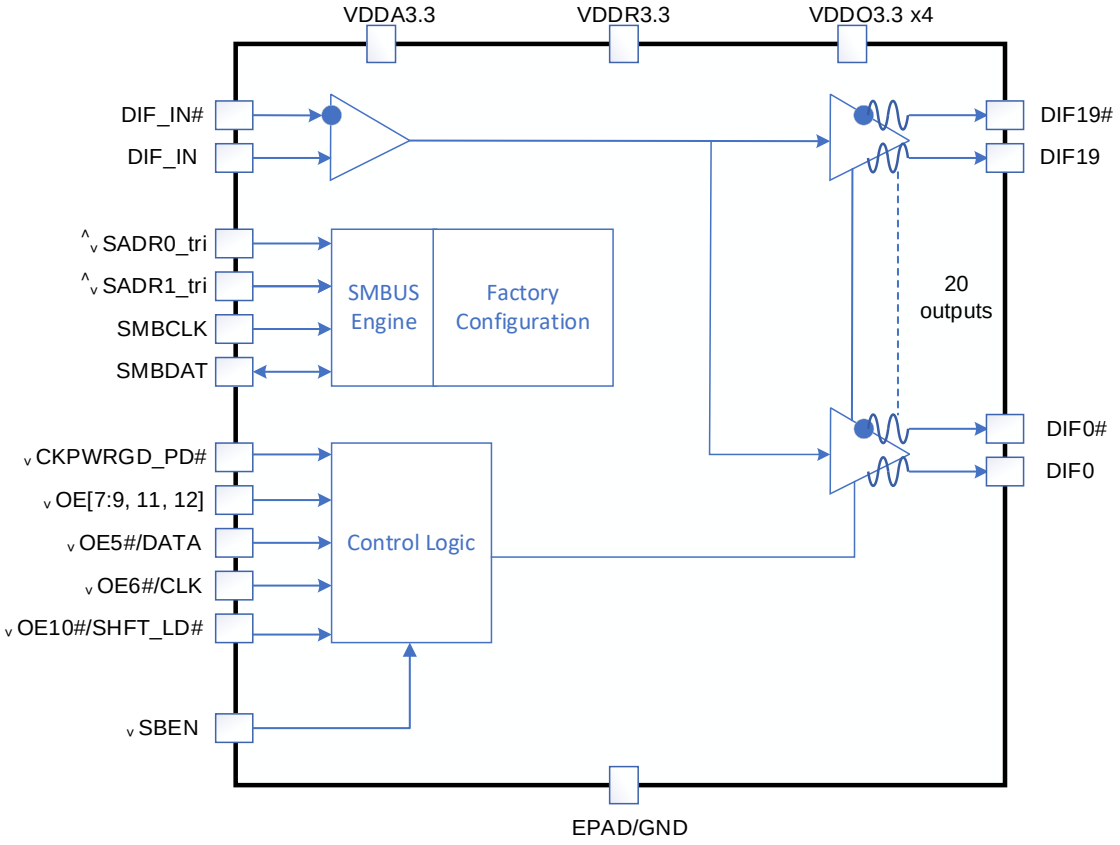
2. Applications

- IT infrastructure (servers, storages)
- 5G communication
- Network system, including switches and routers
- Automotive electronics
- Hardware accelerator

3. Key Features

- Supports Intel's DB2000QL spec
- 3.3-V core and IO supply voltages
- HCSL input: 100MHz (typ), up to 400MHz
- 20 differential low-power HCSL outputs with on-chip termination
- Two output enable control modes
- Traditional 8 OE# pins with power down tolerance and 20 SMBus bits
- Simple 3-wire Side-Band interface real-time control
- SMBus interface support
- 9 selectable SMBus addresses
- Spread spectrum tolerant
- Very low jitter outputs
- Differential additive phase jitter: DB2000Q<30fs RMS
- Differential additive phase jitter: PCIe 4.0<30fs RMS
- Differential additive phase jitter: PCIe 5.0<20fs RMS
- PCIe 1.0/2.0/3.0/4.0/5.0 compliant
- Cycle-to-cycle jitter < 50 ps
- Differential output-to-output skew < 50 ps
- Low propagation delay <3 ns
- Industrial temperature support: -40°C to 85°C
- 6 × 6 mm dual-row LGA80 package

4. Functional Diagram



5. Pin Maps

	1	2	3	4	5	6	7	8	9	10	11	12	
A	DIF17	DIF16#	DIF16	DIF15#	DIF15	DIF14#	DIF14	DIF13#	DIF13	DIF12#	DIF12	DIF11#	A
B	DIF17#	VDDO3.3	NC	^vSADDR0_tri	NC	VDDA3.3	NC	^vSADDR1_tri	NC	vOE12#	VDD3.3	DIF11	B
C	DIF18	NC									vOE11#	DIF10#	C
D	DIF18#	NC									NC	DIF10	D
E	DIF19	vSBEN									vOE10#/SHFT_LD#	vOE9#	E
F	DIF19#	NC									NC	DIF9#	F
G	DIF_IN	NC									NC	DIF9	G
H	DIF_IN#	VDDR3.3									vOE8#	DIF8#	H
J	DIF0	NC									NC	DIF8	J
K	DIF0#	NC									vOE7#	DIF7#	K
L	DIF1	VDDO3.3	NC	SMBDAT	SMBCLK	NC	NC	vOE5#/DATA	NC	vOE6#/CLK	VDDO3.3	DIF7	L
M	DIF1#	DIF2	DIF2#	DIF3	DIF3#	vCKPWRGD_PD#	DIF4	DIF4#	DIF5	DIF5#	DIF6	DIF6#	M
	1	2	3	4	5	6	7	8	9	10	11	12	

TBUF0320
6 x 6 x 0.5mm pitch
LGA80 Package
Top View
EPAD is GND

Figure 1. Pin Assignments for 6 × 6 mm LGQA80 Package – Top View

Note:

a) Pins with ^ prefix have internal pull-up resistor.

b) Pins with v prefix have internal pull-down resistor.

c) Pins with ^v prefix have internal pull-up/pull-down resistor network biasing input to VDD/2.

6. Pin Descriptions

Table 1 Pin Descriptions

Pin #		Pin Name	Type	Description
J	12	DIF8	OUTPUT	Differential true clock output
K	1	DIF0#	OUTPUT	Differential complementary clock output.
K	2	NC	-	No connection.
K	11	vOE7#	INPUT	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
K	12	DIF7#	OUTPUT	Differential complementary clock output.
L	1	DIF1	OUTPUT	Differential true clock output
L	2	VDDO3.3	POWER	Power supply for outputs. Nominally 3.3V.
L	3	NC	-	No connection.
L	4	SMBDAT	I/O	Data pin of SMBUS circuitry.
L	5	SMBCLK	INPUT	Clock pin of SMBUS circuitry
L	6	NC	-	No connection.
L	7	NC	-	No connection.
L	8	vOE5#/DATA	INPUT	Active low input for enabling output 5 or the data pin for the Side-Band Interface. Refer to the **Side-Band Interface** section for details. This pin has an internal pull-down. **OE mode**: 1 = disable output, 0 = enable output. **Side-Band mode**: Data pin.
L	9	NC	-	No connection.
L	10	vOE6#/CLK	INPUT	Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. Refer to the **Side-Band Interface** section for details. This pin has an internal pull-down. **OE mode**: 1 = disable output, 0 = enable output. **Side Band mode**: Clocks data into the Side-Band Interface shift register on the rising edge
L	11	VDDO3.3	POWER	Power supply for outputs. Nominally 3.3V.
L	12	DIF7	OUTPUT	Differential true clock output
M	1	DIF1#	OUTPUT	Differential complementary clock output.
M	2	DIF2	OUTPUT	Differential true clock output
M	3	DIF2#	OUTPUT	Differential complementary clock output.
M	4	DIF3	OUTPUT	Differential true clock output
M	5	DIF3#	OUTPUT	Differential complementary clock output.
M	6	vCKPWRGD_PD#	INPUT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor.
M	7	DIF4	OUTPUT	Differential true clock output
M	8	DIF4#	OUTPUT	Differential complementary clock output.
M	9	DIF5	OUTPUT	Differential true clock output

M	10	DIF5#	OUTPUT	Differential complementary clock output.
M	11	DIF6	OUTPUT	Differential true clock output
M	12	DIF6#	OUTPUT	Differential complementary clock output.
-		EPAD	GND	Connect EPAD to ground